SENSOR SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SAME

FIELD OF THE INVENTION

[0001] The present invention relates in general to integrated circuit packaging, and more particularly to an integrated circuit package for micro electro-mechanical systems integrated circuit chips and a method of manufacturing the same.

BACKGROUND OF THE INVENTION

[0002] High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by industry demands for increased thermal and electrical performance and decreased size and cost of manufacture.

[0003] Micro electro-mechanical systems (MEMS) integrated circuit chips and micro optic electro-mechanical (MOEMS) integrated circuit chips (all generally referred to herein as MEMS) are unique chips used in a variety of applications. MEMS chips commonly include sensors for the detection of signals, such as motion, light, sound, pressure, chemical, radio waves, etc. and are generally employed in carrying out specific tasks based on programmable logic.

[0004] Improvements in integrated circuit packages including MEMS chips are driven by traditional industry demands as well as additional demands for properties that are uniquely desirable for MEMS packages. Some of these desired properties for MEMS packaging include, for example, high chip placement accuracy for MEMS packages used in photonics, effective signal transmission to the sensor area of the MEMS chip, and good isolation of the sensor area of the MEMS chip from packaging materials for protection against stress, freedom of movement for parts of motion sensing chips, and protection of the sensor against damage. Other desirable properties include high mechanical rigidity, high degree of die cleanliness and good reliability.

[0005] In the past, MEMS integrated circuit packages have been manufactured in several different ways. These packages have limitations, however, such as low cost-effectiveness, die placement accuracy, signal transmission and other limitations.

[0006] It is desirable to provide a MEMS integrated circuit package with improved properties desirable in MEMS and optical sensor packages.

SUMMARY OF THE INVENTION

[0007] In one aspect of the present invention, there is provided a process for fabricating an integrated circuit package. The process includes: providing a substrate having conductive traces therein, the substrate also having a cavity therein; mounting a semiconductor die to a first surface of the substrate, in a flip-chip orientation such that a sensor portion of the semiconductor die is aligned with the cavity and conductive interconnects connect pads of the semiconductor die to the conductive traces of the substrate; filling an area surrounding the interconnects with an underfill material; and mounting a plurality of conductive balls on the first surface of the substrate and in electrical connection with the conductive traces such that ones of the conductive balls are connected to ones of the pads of the semiconductor die via the conductive traces.

[0008] In another aspect of the present invention, there is provided an integrated circuit package. The package includes a substrate having conductive traces therein, the substrate also having a cavity therein. A semiconductor die is mounted to a first surface of the substrate, in a flip-chip orientation such that a sensor portion of the semiconductor die is aligned with the cavity and conductive interconnects connect pads of the semiconductor die to the conductive traces of the substrate. An underfill material surrounds the interconnects. A plurality of conductive balls are disposed on the first surface of the substrate, the conductive balls being electrically connected to the conductive traces such that ones of the conductive balls are connected to ones of the pads of the semiconductor die via the conductive traces.

[0009] Several advantages are realized in aspects of embodiments of the present invention. The flip-chip orientation of the semiconductor die provides high placement accuracy. The process for manufacturing the package permits different media to be placed in contact with the sensor portion of the die for increasing signal transmission while inhibiting signal distortion caused by the packaging media. The underfill material provides protection against stress induced on the interconnect due to thermal mismatch between the die and substrate. Reliability of the package is enhanced by reducing the interface to the die.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The invention will be better understood with reference to the drawings and the following description, in which:

[0011] Figure 1 is a sectional side view of an integrated circuit package according to an embodiment of the present invention;

[0012] Figures 2A to 2E show processing steps for fabricating the integrated circuit package of Figure 1;

[0013] Figures 3A to 3G show processing steps for fabricating an integrated circuit package according to another embodiment of the present invention;

[0014] Figure 4 shows a sectional side view of an integrated circuit package according to still another embodiment of the present invention; and

[0015] Figure 5 shows a sectional side view of an integrated circuit package according to yet another embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0016] Reference is first made to Figure 1, which shows a sectional side view of an integrated circuit package indicated generally by the numeral 20. The integrated circuit package 20 includes a substrate 22 having conductive traces therein. A cavity is disposed in the substrate 22. A semiconductor die 28 is mounted to a first surface 24 of the substrate 22, in a flip-chip orientation such that a sensor portion 30 of the semiconductor die 28 is aligned with the cavity. Conductive interconnects 32 connect pads of the semiconductor die 28 to the conductive traces of the substrate 22. An underfill material 34 surrounds the interconnects 32. A plurality of conductive balls 36 are disposed on the first surface 24 of the substrate 22. The conductive balls 36 are electrically connected to the conductive traces such that ones of the conductive balls 36 are connected to ones of the pads of the semiconductor die 28 via the conductive traces.

[0017] The integrated circuit package 20 will now be described in more detail with reference to Figures 2A to 2E to describe processing steps for fabricating the integrated circuit package 20 in accordance with an embodiment of the present invention. Referring first to Figure 2A, the substrate 22 of a bismaleimidetriazine (BT) resin/glass epoxy printed circuit board is shown. The substrate 22 includes conductive metal or alloy traces than provide conductive paths for signal

transfer. The conductive traces are patterned during manufacture of the substrate 22. The substrate 22 manufacturing and patterning of the conductive traces are well known and will be well understood by those skilled in the art. The substrate 22 also includes the cavity that is formed using known techniques during manufacture of the substrate 22 and extends through the thickness of the substrate 22, from the first surface 24 to an opposing second surface 26.

[0018] The substrate 22 is in the form of a strip for producing a number of integrated circuit packages 20. Only one such unit is depicted in Figures 2A to 2E, portions of adjacent units being shown by stippled lines. The present discussion refers to the fabrication of a single integrated circuit package 20 for the purpose of simplicity only and it will be understood that the package 20 is preferably gang fabricated.

[0019] Referring now to Figure 2B, the semiconductor die 28 is then mounted in a flip-chip orientation by connection of the pads of the semiconductor die 28 to the conductive traces of the substrate 22 with the conductive interconnects 32. To mount the semiconductor die 28, solder balls, which form the conductive interconnects 32, are disposed on the semiconductor die 28, using any of the established techniques available in the industry. The semiconductor die 28 is then mounted on the substrate 22 via the conductive interconnects such that the sensor portion 30 of the semiconductor die 28 is aligned with the cavity of the substrate 22, as shown. It will be appreciated that the pads of the semiconductor die 28 align with the portions of the conductive traces and the conductive interconnects 32 electrically connect the semiconductor die 28 with ones of the conductive traces of the substrate 22.

[0020] The area around the conductive interconnects 32 is then filled with a thermosetting polymer, referred to above as the underfill material 34. The underfill material 34 surrounds the interconnects 32 and fills the area between the semiconductor die 28 and the substrate 22, as shown in Figure 2C. Care is taken to inhibit the underfill material 34 from covering the sensor portion 30 of the semiconductor die 30, leaving the sensor portion 30 exposed to air.

[0021] Next, the plurality of conductive balls 36, commonly referred to as solder bumps, are placed on the first surface 24 of the substrate 22, in connection with ones of the conductive traces of the substrate 22, by conventional positioning (Figure 2D). To attach the conductive balls 36, a flux is added to the conductive balls 36 prior to placement and, after placement, the balls 36 are reflowed using known reflow techniques. The conductive balls 36 are thereby connected to the conductive traces of the substrate 22 and through the interconnects 32, to the semiconductor die 26. The conductive balls 36 provide signal and power connections as well as

ground connections for the semiconductor die 28. Clearly the conductive balls 36 are suitably sized to provide clearance between a back side of the semiconductor die 28 and a printed circuit board surface (not shown) when the package 20 is mounted on a printed circuit board.

[0022] Singulation of the individual integrated circuit package 20 from the strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 2E. Thus, the individual package 20 is isolated from other packages of the strip.

[0023] Reference is now made to Figures 3A to 3G to describe a process for manufacturing an integrated circuit package 20 according to another embodiment of the present invention. Figures 3A to 3C are similar to Figures 2A to 2C and therefore are not further described herein. As in the first described embodiment, a plurality of conductive balls 36 are placed on the first surface 24 of the substrate 22, in connection with ones of the conductive traces of the substrate 22, by conventional positioning (Figure 3D). To attach the conductive balls 36, a flux is added to the conductive balls 36 prior to placement and, after placement, the balls 36 are reflowed using known reflow techniques. The conductive balls 36 are thereby connected to the conductive traces of the substrate 22 and through the interconnects 32, to the semiconductor die 26. In the present embodiment, however, the conductive balls 36 serve as I/O (input/output) redistribution balls, rather than serving as second level interconnects. The conductive balls 36 are suitably sized to provide appropriate stand-off for the semiconductor die 28.

[0024] Referring to Figure 3E, the back side of the semiconductor die 28 and the conductive balls 36 (I/O redistribution balls) are encapsulated in an overmold compound 38 such that the conductive balls 36 are exposed at a surface thereof, for providing a connection surface for attaching second level interconnect balls 40. Next, the second level interconnect balls 40 are attached to the exposed surfaces of the conductive balls 36 by conventional positioning techniques (Figure 3F). In the present embodiment, the second level interconnect balls 40 are electrically connected to the semiconductor die 28 via the conductive balls 36, the conductive traces of the substrate 22 and the interconnects 32.

[0025] Singulation of the individual integrated circuit package 20 from the strip is then performed either by saw singulation or die punching, resulting in the configuration shown in Figure 3G. Thus, the individual package 20 is isolated from other packages of the strip.

[0026] Several variations and modifications can be made to the embodiments described herein. An alternative embodiment of the package is shown in Figure 4 in which the underfill

material 34 covers the sensor portion 30 of the semiconductor die 30 rather than leaving the sensor portion 30 exposed to air. Thus, the sensor portion 30 of the semiconductor die 28 is covered with the polymeric underfill material 34 or other material suitable for the package 20 being manufactured.

[0027] In another embodiment, a lid 42 of, for example, glass is attached to the second surface 26 of the substrate 22, thereby covering and protecting the sensor portion 30 of the semiconductor die 28, as shown in Figure 5. The lid 42 is attached to the surface of the substrate 22 after underfilling with the underfill material 34, as shown in Figure 2C. In this embodiment, a cleaning step is added to remove possible contamination of the semiconductor die 28, prior to attaching the lid 42. The lid is then immediately attached to inhibit any contamination from the environment or assembly process from settling on the semiconductor die 28. Thus, the lid 42 protects the surface of the sensor portion 30 of the semiconductor die 28.

[0028] Other materials can be used to cover the sensor portion 30 of the semiconductor die 28, depending on the intended application of the integrated circuit package 20. These materials are used, for example, for light filters, stress absorbers, ionic corrosion protection or many other functions. For example, for photonic applications, the sensor portion 30 is covered with either air accompanied by a glass lid or with a transparent encapsulant. In other exemplary applications, light filters are also employed. Clearly, transmission is an important aspect and appropriate materials are selected to inhibit selective blocking of desired wavelengths by package media. For a pressure sensor application, the sensor portion 30 is covered either with air or with a low stress encapsulant. In this application, appropriate materials are selected to inhibit thermally variable stresses exerted by packaging media on the die and to inhibit pressure damping by the material. A motion sensor includes moveable parts and for this application the sensor portion 30 is covered by air.

[0029] Specific embodiments and variations of embodiments of the present invention have been shown and described herein. However, other variations and modifications to these embodiments may occur to those skilled in the art. For example, the substrate 22 is not limited to the BT resin/glass epoxy printed circuit board as described and other suitable substrate materials can be employed. Also, the conductive interconnects 32 are not limited to solder ball conductive interconnects, as described. Other conductive interconnect materials can be used, including, for example, gold, copper, aluminum and conductive polymers.

[0030] Still other variations and modifications may occur to those skilled in the art. All such modifications and variations are believed to be within the sphere and scope of the present invention.